

**REMARKS**

Claims 1-5, 7-10, 21, 23-26, and 28-30 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the above amendments and following remarks.

Claims 1-5, 7-10, 21, 23-26, and 28-30 were rejected under 35 U.S.C. § 112, first paragraph.

The amendments to the claims obviate the rejections to these claims.

Claims 1-5, 7-10, 21, 23-26, and 28-30 are in full compliance with § 112.

Turning now to the art rejection, Claims 1, 3-5, 7, 8, 10, 21, 23-26, and 28-30 were rejected under 35 U.S.C. § 102(a) as being anticipated by Derderian; and Claims 2 and 9 were rejected under 35 U.S.C. § 103 as being obvious over Derderian.

These rejections are respectfully traversed.

It is respectfully submitted that Derderian does not disclose or suggest the presently claimed invention including a first attached layer to directly couple the first chip and the second chip in the various forms in independent Claims 1 and 21.

The Examiner's attention is directed to Figure 9 of Derderian where spacers 22 area shown. The spacers result in a higher profile combination.

It is respectfully submitted that Claims 1-5, 7-10, 21, 23-26, and 28-30 are allowable over the applied art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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